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10/015,229	12/13/2001	Prashanth Kumar Adamane	AUS920010350US1	6261

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EXAMINER

DAMIANO, ANNE L

ART UNIT	PAPER NUMBER
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2114

3

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/015,229

Applicant(s)

ADAMANE ET AL.

Examiner

Anne L. Damiano

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/13/01.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 11-19, 22-31 and 34-36 is/are rejected.
- 7) ☒ Claim(s) 9, 10, 20, 21, 32 and 33 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Art Unit: 2114

DETAILED ACTION

Allowable Subject Matter

1. Claims 9, 10, 20, 21, 32 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 36 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The phrase "test nanokernel" is not mentioned in the entire application besides in claim 36.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2114

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-6-8, 12, 14-19, 23, 24, 26-31 and 35 are rejected under 35

U.S.C. 102(b) as being anticipated by Jennings (6,110,218).

As in claim 1, Jennings discloses a method operative in an input/output device associated with a computer system, comprising:

Performing a plurality of direct memory access transfers with respect to memory of the computer system, wherein parameters (attributes) of the direct memory access transfers are varied pseudo-randomly (column 1: lines 55-60, column 2: lines 7-8, column 3: lines 46-50, lines 60-64, column 5: lines 25-29, column 6: lines 7-38). (The system performs a number of different test cycles on a design under test, said tests including a DMA test cycle. The design under test is passed parameters indicating the type of DMA test cycle by the random cycle description generator. The parameters are generated by the random cycle test generator (column 3: lines 60-65) and are varied randomly (column 5: lines 25-30).)

As in claim 3, Jennings discloses the method of claim 1, wherein the parameters include transfer size (column 5: lines 25-29).

As in claim 4, Jennings discloses the method of claim 1, wherein the parameters include at least one of transfer width and byte lane enables (column 5: lines 25-29).

As in claim 5, Jennings discloses the method of claim 1, wherein the parameters include at least one of request assertion time, request deassertion time, number of wait states, number of idle states (breakup frequency), disconnect count, retry limit, and whether to override a latency timer (column 5: lines 25-29).

As in claim 6, Jennings discloses the method of claim 1, further including performing additional bus commands (column 1: line 66-column 2: line 4). (Another random cycle being selected involves additional bus commands.)

As in claim 7, Jennings discloses the method of claim 6, wherein the additional bus commands include all possible bus commands (column 1: line 66-column 2: line 4). (Another random cycle being selected involves additional bus commands, interpreted as being all that are possible at the given time.)

As in claim 8, Jennings discloses the method of claim 1, wherein the direct memory transfers are performed concurrently with memory accesses by a processor in the computer system (column 6: lines 7-38). (While the DMA controller is being configured and the direct memory transfers are being performed, the memory is accessed (column 6: lines 27-32).)

Art Unit: 2114

As in claim 12, Jennings discloses a computer program product in a computer readable medium and operative in an input/output device associated with a computer system, comprising functional descriptive material that when processed by an input/output device (The design under test is an I/O device), enables the input/output device to perform acts of:

Performing a plurality of direct memory access transfers with respect to memory of the computer system, wherein parameters of the direct memory access transfers are varied pseudo-randomly (column 1: lines 55-60, column 2: lines 7-8, column 3: lines 46-50, lines 60-64, column 5: lines 25-29, column 6: lines 7-38). (The system performs a number of different test cycles on a design under test, said tests including a DMA test cycle. The design under test is passed parameters indicating the type of DMA test cycle by the random cycle description generator. The parameters are generated by the random cycle test generator (column 3: lines 60-65) and are varied randomly (column 5: lines 25-30).)

As in claim 14, Jennings discloses the computer program product of claim 12, wherein the parameters include transfer size (column 5: lines 25-29).

As in claim 15, Jennings discloses the computer program product of claim 12, wherein the parameters include at least one of transfer width and byte lane enables (column 5: lines 25-29).

Art Unit: 2114

As in claim 16, Jennings discloses the computer program product of claim 12, wherein the parameters include at least one of request assertion time, request deassertion time, number of wait states, number of idle states (breakup frequency), disconnect count, retry limit, and whether to override a latency timer (column 5: lines 25-29).

As in claim 17, Jennings discloses the computer program product of claim 12, wherein the functional descriptive material enables the computer to perform additional acts including performing additional bus commands (column 1: line 66-column 2: line 4). (Another random cycle being selected involves additional bus commands.)

As in claim 18, Jennings discloses the computer program product of claim 17, wherein the additional bus commands include all possible bus commands (column 1: line 66-column 2: line 4). (Another random cycle being selected involves additional bus commands, interpreted as being all that are possible at the given time.)

As in claim 19, Jennings the computer program product of claim 12, wherein the direct memory transfers are performed concurrently with memory accesses by a processor in the computer system (column 6: lines 7-38). (While the DMA controller is being configured and the direct memory transfers are being performed, the memory is accessed (column 6: lines 27-32).)

Art Unit: 2114

As in claim 23, Jennings discloses a computer program product in a computer readable medium comprising functional descriptive material that when processed by an input/output device, enables the input/output device to perform acts of:

Directing the at least one peripheral device (design under test) (column 2: lines 65-67) to perform direct memory access transfers with respect to the memory and with pseudo-random variations in direct memory access transfer parameters (column 1: lines 55-60, column 2: lines 7-8, column 3: lines 46-50, lines 60-64, column 5: lines 25-29, column 6: lines 7-38); (The system performs a number of different test cycles on a design under test, said tests including a DMA test cycle. The design under test is passed parameters indicating the type of DMA test cycle by the random cycle description generator. The parameters are generated by the random cycle test generator (column 3: lines 60-65) and are varied randomly (column 5: lines 25-30).)

Accessing a portion of the memory concurrently with the at least one peripheral device (column 6: lines 7-38). (While the DMA controller is being configured, the memory is accessed (lines 27-32)).

As in claim 24, Jennings discloses an input/output device (design under test) comprising means for: performing a plurality of direct memory access transfers with respect to memory of a computer system, wherein parameters of the direct memory access transfers are varied pseudo-randomly (column 1: lines 55-60, column 2: lines 7-8, column 3: lines 46-50, lines 60-64, column 5: lines 25-29, column 6: lines 7-38).

Art Unit: 2114

As in claim 26, Jennings discloses the input/output device of claim 24, wherein the parameters include transfer size (column 5: lines 25-30).

As in claim 27, Jennings discloses the input/output device of claim 24, wherein the parameters include at least one of transfer width and byte lane enables (column 5: lines 25-30).

As in claim 28, Jennings discloses the input/output device of claim 24, wherein the parameters include at least one of request assertion time, request deassertion time, number of wait states, number of idle states (breakup frequency), disconnect count, retry limit, and whether to override a latency timer (column 5: lines 25-30).

As in claim 29, Jennings discloses the input/output device of claim 24, further comprising means for performing additional bus commands (column 1: line 66-column 2: line 4). (Another random cycle being selected involves additional bus commands.)

As in claim 30, Jennings discloses the input/output device of claim 29, wherein the additional bus commands include all possible bus commands (column 1: line 66-column 2: line 4). (Another random cycle being selected involves additional bus commands, interpreted as being all that are possible at the given time.)

As in claim 31, Jennings discloses the input/output device of claim 24, wherein the direct-memory transfers are performed-concurrently with memory accesses by a

Art Unit: 2114

processor in the computer system (column 6: lines 7-38). (While the DMA controller is being configured and the direct memory transfers are being performed, the memory is accessed (column 6: lines 27-32).)

As in claim 35, Jennings discloses a computer system comprising:

Memory (figure 1B: component 9 and column 3: lines 2-6);

At least one peripheral device (Design under test) configured to be able to access the memory (memory is part of dut.);

At least one processor associated with the memory (figure 1B: component 12 and column 3: lines 1-2); and

Functional descriptive material within the memory, wherein the at least one processor processes the functional descriptive material to perform acts of (column 3: lines 1-6):

Directing the at least one peripheral device to perform direct memory access transfers with respect to the memory and with pseudo-random variations in direct memory access transfer parameters (column 1: lines 55-60, column 2: lines 7-8, column 3: lines 46-50, lines 60-64, column 5: lines 25-29, column 6: lines 7-38); (The system performs a number of different test cycles on a design under test, said tests including a DMA test cycle. The design under test is passed parameters indicating the type of test cycle by the random cycle description generator. The parameters are generated by the random cycle test generator (column 3: lines 60-65).)

Art Unit: 2114

And accessing a portion of the memory concurrently with the at least one peripheral device (column 6: lines 7-38). (While the DMA controller is being configured, the memory is accessed (lines 27-32)).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 2, 11, 13, 22, 25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennings as applied to claims 1, 12 and 24 above.

Regarding claims 2, 13 and 25, Jennings discloses performing a plurality of DMA transfers with the parameters varying randomly above. Jennings also discloses different examples of the variations of the different parameters including transfer type and size (column 5: lines 25-29). However, Jennings does not specifically disclose the parameter variations including the start address alignment.

It would have been obvious to a person skilled in the art at the time the invention was made to include the start address alignment in the variation of parameters in the system taught by Jennings. It would have been obvious because a start address is required as a parameter for a memory access. A person skilled in the art would have

Art Unit: 2114

understood that although not specifically discloses Jennings meant for the start address alignment to be included in the listing of parameter variations.

Regarding claims 11, 22, and 34 Jennings discloses performing a plurality of direct memory access transfers with respect to memory of a computer system above. However, Jennings does not specifically disclose the memory including a cache memory.

It would have been obvious to a person skilled in the art at the time the invention was made to include a cache memory in the system taught by Jennings. It would have been obvious because system memories generally include caches that would be associated or related to the memory with which the DMA transfers are occurring in Jennings' system. A person skilled in the art would have understood that although not specifically disclosed, the memory of Jennings system included a cache.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

ALD


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

Art Unit: 2114

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD



SCOTT BADERMAN
PRIMARY EXAMINER